Abstract

Typically, for processing systems it must be guaranteed that all interrupted program stream parameters are restored before the execution of the first program stream resumes. If during this transfer an interrupt occurs, then all data may not be stored or restored. If the error free storage of the program register contents and other critical first program stream data does not occur, the processor (180) has no way of knowing whether the first program stream data restored to the registers has become corrupt or not. Thus, a novel register architecture (120, 121, 122, 123, 124, 125) is provided that facilitate processing of interrupting program streams without storing and restoring interrupted program stream critical data.